

Title: High Latency Interface Between Hardware Components Inventor: Saeed Azimi, Serial No.: 09/661912 Filing Date: September 14, 2000 REPLACEMENT SHEET

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FIG. 1

(Prior Art)

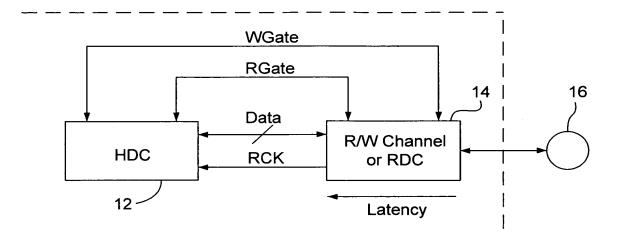
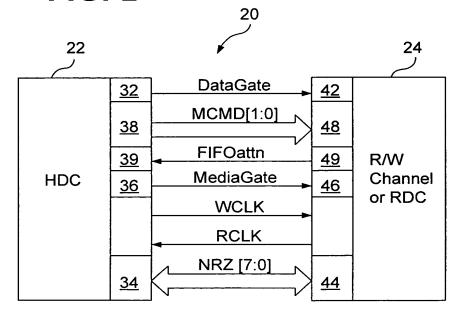


FIG. 2







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FIG. 3

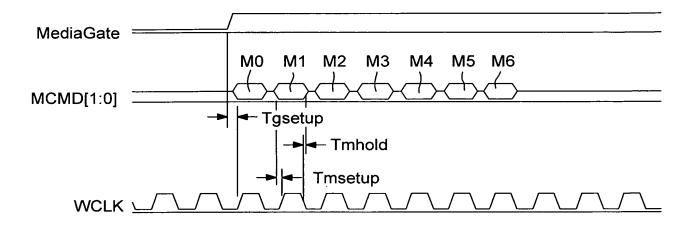


FIG. 4a

Servo				
	P¸LO	User _, Da	ata	ŞW
Track		$\mathcal{M} \setminus \mathcal{M}$	$\Box X \subset X X \Sigma \Box$	
MediaGate		User Data	PÁD (C	Sector 3
			<u>\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\</u>	
MCMD[1:0]				
	\\\			
WCLK				
DataGate				
DataGate				
FIFOattn				
NRZ	— <u>0111</u> - <u><11010001111110000111111100</u>		55	



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FIG. 4b

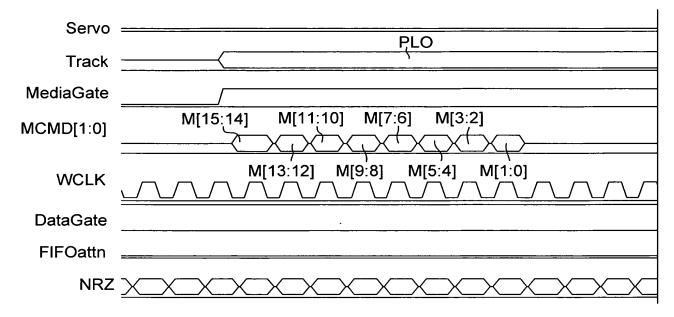


FIG. 4c

Santa	
Servo	
Track	
MediaGate	
MCMD[1·0]	
WCLK	
DataGate	
FIFOattn	
i ii Oattii	DCMD D0 D1 D2 DCMD D3 D4 D5
NRZ	



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FIG. 5a

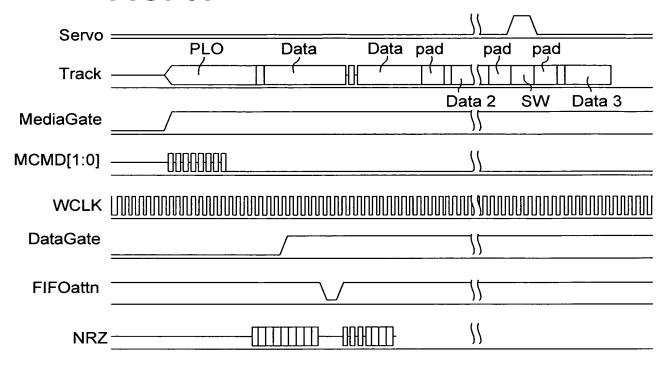
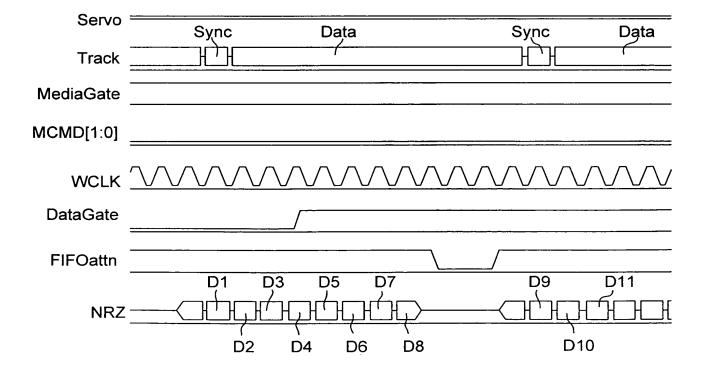


FIG. 5b





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FIG. 5c

Servo		
Gervo	PLO	Sync
Track		
MediaGate		
MCMD[1:0]		
WCLK	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	$\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{$
DataGate		
FIFOattn		
		D ₁ D ₂
NRZ		